epitaxial growth of the second portion 20B of the second layer 20.

As shown in FIG. 6B, thereafter, a first window 42 is opened through the first protective layer to expose a first portion 44 of the surface of the second layer 20 of the semiconductor device 10. The exposed surface portion 44 of the second layer 20 is doped with a heavy concentration of one type conductivity dopants such as boron dopants by, for instance, implantation of diffusion techniques to establish a first portion 26 of the first region 24 comprising a heavy concentration of one type conductivity carriers.

Thereafter, and as shown in FIG. 6C, a second mask is used to open a second window 48 through the first protective layer 40 to expose a second surface portion 50 of the surface of the second layer 20. The second surface portion 50 circumscribes and encompasses the first portion 44 of the second layer 20. Thereafter, a moderate concentration of one type conductivity impurities such as boron impurities is introduced by, for instance, implantation or diffusion techniques into the second layer 20 and the first portion 26 of the first region 24 to establish a second portion 28 of the first region 24. The second portion 24 extends to a depth which is less than the depth of the first portion 26 of the first region 24 and partially latterally surrounds the first portion 26 of the first region 24. The second portion 26 is also less heavily doped that the first region 28.

Thereafter, and as shown in FIG. 6D, a second protective layer 54 such as a silicon oxide layer 54 is formed within the second window 48.

Thereafter and as shown in FIG. 6E, a third annular or ring-shaped window 64 is opened through the second protective layer 54 to expose a third surface portion 66 of the surface 21 of the device 10. Thereafter, opposite type conductivity dopants such as arsenic dopants are introduced through the third window 64 into the first region 24 to establish a second region 34 of opposite type conductivity.

As shown in FIG. 6F, a third protective layer 70 such as a silicon dioxide layer is formed within the third window 64. Thereafter, and as shown in FIG. 4G, a fourth window 74 is opened through the second protective layer 54 and a portion of the third protective layer 70.

As shown in FIG. 6H, a metallization layer 76 such as aluminum is deposited within the fourth window 74 on the first surface to establish a cathode electrode 32 in ohmic contact with the first and second regions 24 and 34, respectively. In addition, the metal layer 76 is applied over the insulation layer 70 to provide a gate electrode material 78 such as a metal. The gate material can be selected from the group comprising polysilicon, polysilicide and refractory metals. Tungsten is preferably deposited over the first insulation layer 40 and possibly a portion of the third insulation layer 70. The gate electrode material 78 thus overlies a second portion 28 of the first region 24 as well as a portion of the second region 34 and the second layer 20.

It is preferred that the first region 24 be doped and driven in relation to the grid 22 so that in one embodiment, the first region 24 overlaps onto a portion of the grid 22 and in alternate embodiment, so that a region 22*b* of the grid 22 remains discrete and separated by the second layer 20 from the first region 24 to establish a separate grid region 22*b* of one type conductivity within the device.

In a preferred embodiment, a separate electrode 30 is provided to the heavily doped grid 22 by, for instance, providing a sinker region 80 of one type conductivity making contact with the grid 22, and providing a metallized contact within an extremity of the device to establish direct electrical connection to the heavily doped grid of the device. Electrical contact can also be established between the grid electrode 30 and the cathode electrode 22 to provide two cathode current paths for one type conductivity carriers.

It is to be recognized that while the preferred embodiments of the present invention have been disclosed with respect to an insulated gate transistor, the extra short grid of the present invention is equally applicable to other insulated gate semiconductor devices. Further, it is to be recognized that the inclusion of the extra short grid of the present invention within the insulated gate semiconductor device improves not only the latching threshold of the device, but also provides for improvements in other operating characteristics such as turn-off capability.

While preferred embodiment of the present invention have been illustrated and described, it is clear that the invention is not so limited. Numerous modifications and changes, variations and substitutions and equivalents will occur to those skilled in the art without departing from the true spirit and scope of the present invention. Accordingly, it is intended that the invention herein be limited only be scope of the appended claims.

What is claimed is:

1. An insulated gate semiconductor device comprising:

a body of semiconductor material including:

a first layer of one type conductivity,

a second layer of opposite type conductivity disposed atop said first layer,

a first region of one type conductivity within said second layer,

a second region of opposite type conductivity disposed within said first region,

said body having a first surface to which said second layer, said first region and said second region extend, and

a heavily doped grid of one type conductivity disposed within said second layer and spaced from said first surface for establishing a current path for one type conductivity carriers, said grid comprising a plurality of segments of one type conductivity disposed in a substantially planar arrangement and a plurality of aperture therebetween each occupied at least in part by a portion of said opposite type conductivity second layer, at least one of said grid segments and at least one of said grid apertures in projection on said first surface extending into a projection of said first region on said first surface;

a first power electrode disposed in ohmic contact with said first layer;

a second power electrode disposed in ohmic contact with said first and second regions; and

an insulated gate electrode disposed on said first surface over a portion of said first region for, in response to an appropriate bias potential, establishing a channel through said first region between said second layer and said second region for facilitating the flow of opposite type conductivity carriers between said second layer and said second region;